REMARKS

In response to the Office Action mailed June 28, 2004, applicant respectfully requests reconsideration. In the Office Action, claims 5, 6, 9 and 21 were objected to and claims 1-24 were rejected. By this amendment, claims 1, 3-6, 9-11, 13 and 21-23 have been amended. Claims 1-24 remain pending in the application.

Objection to Claims

Claims 5, 6, 9 and 21 were objected to because of various informalities.

Regarding claim 5, the examiner stated that the claim was unclear as to what was being invalidated. Amended claim 5 recites, in part, that "the I/O controller causes a data transfer occurring contemporaneously with the testing of the SUT to be invalidated." Applicant is not quite sure what is unclear about this claim. As stated in the claim, a data transfer occurring contemporaneously with the testing of the SUT is caused to be invalidated.

Regarding claim 6, the examiner states that the claim language does not describe or make clear which of the two control signals may be selected. Amended claim 6 recites, in part, "wherein the respective assertion state of the one of the two control signals is selected."

Claim 1, from which claim 6 depends, recites two control signals, "one of the two control signals being transmitted to the third logic section from a source that is external to the SUT,..." and "the other of the two control signals being transmitted to the third logic section from the first logic section...." The control signal referred to in claim 6 is the "one of the two" rather than "the other of the two."

Regarding claims 9 and 21, the examiner states that it is not clear how the second logic section may be used in causing the memory to store an erroneous value. Claims 9 and 21 have been amended to make the operation of the second logic section more clear.

Claim Rejections Under 35 U.S.C. §112

Claims 1, 3-6, 9, 10, 13, 21 and 22 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite.

Claims 1, 3-6, 9, 10, 13, 21 and 22 have been amended generally as suggested by the examiner, thereby rendering this rejection moot.

Claims 11 and 23 were 22 were rejected under 35 U.S.C. §112, second paragraph, for having insufficient antecedent basis. The examiner states that the limitation "the source" is external to the ASIC and therefore there is insufficient antecedent basis for the limitation in each claim.

This rejection is respectfully traversed, as there is antecedent basis for "the source" in each independent claim from which the rejected claims depend. Regarding claim 11, independent claim 10 recites, beginning on line 11, "a source that is external to the plurality of systems-under-test, the first logic section, the plurality of second logic sections, and the plurality of third logic sections...." Therefore, the recitation of "the source" in claim 11 has sufficient antecedent basis.

Likewise, independent claim 22 recites, beginning on line 10, "a source that is external to the plurality of systems-under-test, the first logic section, the plurality of second logic sections, and the plurality of third logic sections...." Accordingly, the recitation of "the source" in claim 23 has sufficient antecedent basis.

Claim Rejections Under 35 U.S.C. §103

Claims 1-24 were rejected under 35 U.S.C. §103(a) as being unpatentable over Irrinki et al. in view of Lattimore et al. The examiner claims that Irrinki teaches a first logic section (BIST Unit 120), a second logic section (Control Block 130) and a third logic section (multiplexers 250 and 252). The examiner states that "Irrinki does not explicitly teach that multiplexers 250 and 252 selectively couples the first the BIST unit 120 (first logic section) and control block 130 (second logic section)." The examiner also states that "Irrinki does teach the address multiplexer 250 (third logic section) selects between address 132 from the external pins and BIST address 232 (based on BIST select 124)(transmitted from the first logic section)," and that, based on the teachings of Lattimore, that it would have obvious to one of ordinary skill in the art to modify Irrinki's control block 130 (second logic unit) to couple Lattimore's bus interface unit (BIU) 401 and CPU 404 to Irrinki's multiplexer 250. The examiner supports this assertion by stating that this would enable Irrinki to exercise control of the signal coming from the

external pins during normal mode. As best as applicant can understand this rejection, it is respectfully traversed.

Irrinki teaches a method for testing memory devices during the manufacturing process (Col. 1, lines 10-11). The method includes using BIST 120 for testing for faulty memory cells in an associated memory array 140 during power-up. Upon power-up, BIST unit 120 cycles memory array 140 through various test patterns. Every time a failing row or column is detected by the BIST 120, the information is conveyed to the BISR 110 which attempts to reassign accesses to the failing location to a redundant row or column within the array (Col. 3, lines 58-63). However, the BIST 120 only operates at power-up (Col. 4, lines 6-7; Col. 6, lines 35-36; Col. 7, lines 43-45). When power is applied to memory storage device 100, BIST 120 begins a test algorithm to verify the operation of memory array 140 (Col. 5, lines 20-22). After the BIST 120 has completed its testing, state machine controller 210 of BIST 120 becomes inactive and stops asserting BIST select signal 124. After this occurs, normal operation of the memory array proceeds and address 132 is selected at address multiplexer 250 (Col. 5, lines 52-62). BISR 110 monitors incoming addresses on uncorrected address line 116 to determine if any match one of the failing addresses detected by the BIST 120. If a match is found, BISR 110 conveys the corrected address 114 using corrected address select signal 112 through multiplexer 252 (Col. 3, line 63- col. 4, line 5).

The examiner's interpretation of what is taught is not supported by Irrinki. First, the examiner states that the BIST unit 120 corresponds to the "first logic unit" recited in claim 1, that the control block 130 corresponds to the "second logic unit" and that multiplexers 250 and 252 correspond to the "third logic unit". However, as shown in Fig. 2 and described in Column 5, lines 1-4, multiplexers 250 and 252 are part of the control block 130. Therefore, multiplexers 250 and 252 cannot be both the second logic unit and the third logic unit.

Furthermore, the examiner states that it would have been obvious to modify Irrinki's control block 130 to couple Latimore's bus interface unit 401 and CPU 404 to Irrinki's multiplexer 250 to enable Irrinki to exercise control of the signal coming from the external pins during normal mode. However, there is no need for Irrinki to "control" signals from the external pins during normal operation. Once the BIST 120 becomes

inactive, as described above, the memory device operated normally and the external signals are input through the control block 130 and to the memory array 140, as described above. There is no motivation in Irrinki for the addition of Lattimore's bus interface unit or CPU to Irrinki's multiplexer 250, nor is there motivation for the signals from the external pins to be "controlled" during normal operation. The examiner seems to have taken components from Lattimore and stated that they could be incorporated into Irrinki without considering how the components would be incorporated, why they would be incorporated and what the end result of the incorporation would be. After a thorough reading of Irrinki, it is not clear to the applicant how the Lattimore components suggested by the examiner would be incorporated into Irrinki and what the end result would be. The examiner has provided no support in either reference for the combination. There is no need in Irrinki for the signals to be controlled during normal operation. Therefore, there is no need for the Lattimore components to be incorporated in to Irrinki as suggested by the examiner.

Accordingly, because the combination suggested by the examiner is improper as not being supported by any motivation to combine in either reference, the rejection of claims 1-24 under 35 U.S.C. §103(a) is improper and should be withdrawn.

Furthermore, even if the combination were proper, which applicant asserts that it is not, the combination would not teach the invention recited in claims 1-24. Independent claim 1 recites a testing system for use in testing a system-under-test (SUT), the testing system comprising:

a first logic section that may transmit one or more test-related signals for use during a test mode of the SUT;

a second logic section that may transmit one or more other signals during a normal operating mode of the SUT; and

a third logic section that selectively couples the first logic section or the second logic section to the SUT based upon respective assertion states of two control signals, one of the two control signals being transmitted to the third logic section from a source that is external to the SUT, the first logic section, the second logic section, and the third logic section, the other of the two control signals being transmitted to the third logic section from the first logic section;

wherein:

> when the third logic section couples the first logic section to the SUT, the first logic section transmits the one or more test-related signals to the SUT, and when the third logic section couples the second logic section to the SUT, the second logic section may transmit the one or more other signals to the SUT.

As set forth above, Irrinki does not teach a first logic section, a second logic section and a third logic section. The multiplexers 250, 252 that the examiner states correspond to the third logic circuit in the claim are actually part of the control block 130, which the examiner states corresponds to the second logic section. If the multiplexers are the third logic section, as suggested by the examiner, then Irrinki does not teach a second logic section. If the examiner believes that the control block 130 corresponds to the second logic section, then Irrinki also does not teach a third logic section that selectively couples the first logic section or the second logic section to the SUT based upon respective assertion states of two control signals, as recited in the claim. Lattimore does not add anything that would enable Irrinki to have a first logic section, a second logic section and a third logic section, as recited in independent claim 1.

Furthermore, Irrinki does not teach two control signals. The BIST unit 120 of Irrinki begins its test algorithm when power is applied to memory storage device 100 to verify the operation of memory array 140 (Col. 5, lines 20-22). After the BIST unit 120 has completed testing, it becomes inactive and normal operation of the memory storage device proceeds (Col. 5, lines 52-56). Once normal operation of the memory is underway, the BIST unit 120 is not utilized. Therefore, there is no need for control signals being transmitted to the third logic section (which is not present in Irrinki). Lattimore does not add anything that would enable Irrinki to have two control signals, as recited in independent claim 1.

Since Irrinki does not teach or suggest a first logic section, a second logic section and a third logic section, and the addition of Lattimore does not provide Irrinki with a first logic section, a second logic section and a third logic section, the combination cannot teach or suggest that when the third logic section couples the first logic section to the SUT, the first logic section transmits the one or more test-related signals to the SUT, and

when the third logic section couples the second logic section to the SUT, the second logic section may transmit the one or more other signals to the SUT, as recited in independent claim 1.

Accordingly, since the (improper) combination of Irrinki and Lattimore does not teach or suggest the invention recited in independent claim 1, independent claim 1 is allowable over the combination, and the rejection of independent claim 1 under 35 U.S.C. §103(a) should be withdrawn.

Claims 2-9 depend from independent claim 1 and are allowable for at least the same reasons as independent claim 1.

Independent claim 10 recites a testing system for use in testing a plurality of systems-under-test, the testing system comprising:

a first logic section;

a plurality of second logic sections;

a plurality of third logic sections;

each respective third logic section being coupled to the first logic section and to a respective second logic section, and being configured to selectively couple the first logic section or the respective second logic section to a respective system-under-test based upon a respective control signal from the first logic section and also based upon another control signal, the another control signal being transmitted to each third logic section from a source that is external to the plurality of systems-under-test, the first logic section, the plurality of second logic sections, and the plurality of third logic sections;

wherein:

> when the first logic section is coupled to the respective SUT, the first logic section may transmit one or more test-related signals to the respective SUT, and when the respective second logic section is coupled to the respective SUT, the respective second logic section may transmit one or more respective other signals to the respective SUT.

As set forth above with regard to independent claim 1, Irrinki does not teach a first logic section, a second logic section and a third logic section. It follows then, that Irrinki does not teach a plurality of second logic sections and a plurality of third logic sections. The multiplexers 250, 252 that the examiner states correspond to the third logic

circuit in the claim are actually part of the control block 130, which the examiner states corresponds to the second logic section. If the multiplexers are the third logic section, as suggested by the examiner, then Irrinki does not teach a second logic section. If the examiner believes that the control block 130 corresponds to the second logic section, then Irrinki also does not teach a third logic section that selectively couples the first logic section or the respective second logic section to the respective system-under-test based upon two control signals, as recited in the claim. Lattimore does not add anything that would enable Irrinki to have a first logic section, a plurality of second logic sections and a plurality of third logic sections, as recited in independent claim 10.

Furthermore, Irrinki does not teach two control signals. The BIST unit 120 of Irrinki begins its test algorithm when power is applied to memory storage device 100 to verify the operation of memory array 140 (Col. 5, lines 20-22). After the BIST unit 120 has completed testing, it becomes inactive and normal operation of the memory storage device proceeds (Col. 5, lines 52-56). Once normal operation of the memory is underway, the BIST unit 120 is not utilized. Therefore, there is no need for control signals being transmitted to the third logic section (which is not present in Irrinki). Lattimore does not add anything that would enable Irrinki to have two control signals, as recited in independent claim 10.

Since Irrinki does not teach or suggest a first logic section, a plurality of second logic sections and a plurality of third logic sections, and the addition of Lattimore does not provide Irrinki with a first logic section, a plurality of second logic sections and a plurality of third logic sections, the combination cannot teach or suggest that when the first logic section is coupled to the respective SUT, the first logic section may transmit one or more test-related signals to the respective SUT, and when the respective second logic section is coupled to the respective SUT, the respective second logic section may transmit one or more respective other signals to the respective SUT, as recited in independent claim 10.

Accordingly, since the (improper) combination of Irrinki and Lattimore does not teach or suggest the invention recited in independent claim 10, independent claim 10 is allowable over the combination, and the rejection of independent claim 10 under 35 U.S.C. §103(a) should be withdrawn.

Claims 11 and 12 depend from independent claim 10 and are allowable for at least the same reasons as independent claim 10.

Independent claim 13 recites a method of using a testing system for testing a system-under-test (SUT), the testing system including a first logic section, a second logic section, and a third logic section, the method comprising:

selectively coupling, via the third logic section, the first logic section or the second logic section to the SUT based upon respective assertion states of two control signals, one of the two control signals being transmitted to the third logic section from a source that is external to the SUT, the first logic section, the second logic section, and the third logic section, the other of the two control signals being transmitted to the third logic section from the first logic section;

transmitting to the SUT from the first logic section, when the first logic section is coupled to the SUT via the third logic section, one or more test-related signals; and

transmitting to the SUT from the second logic section, when the second logic section is coupled to the SUT via the third logic section, one or more other signals to the SUT.

As set forth above with regard to independent claim 1, Irrinki does not teach a first logic section, a second logic section and a third logic section. It follows then, that Irrinki does not teach selectively coupling, via the third logic section, the first logic section or the second logic section to the SUT based upon respective assertion states of two control signals. The multiplexers 250, 252 that the examiner states correspond to the third logic circuit in the claim are actually part of the control block 130, which the examiner states corresponds to the second logic section. If the multiplexers are the third logic section, as suggested by the examiner, then Irrinki does not teach a second logic section. If the examiner believes that the control block 130 corresponds to the second logic section, then Irrinki also does not teach a third logic section that selectively couples the first logic section or the second logic section to the SUT based upon two control signals, as recited in the claim. Lattimore does not add anything that would enable Irrinki to have a first logic section, a plurality of second logic sections and a plurality of third logic sections, as recited in independent claim 13.

Furthermore, Irrinki does not teach two control signals. The BIST unit 120 of Irrinki begins its test algorithm when power is applied to memory storage device 100 to verify the operation of memory array 140 (Col. 5, lines 20-22). After the BIST unit 120 has completed testing, it becomes inactive and normal operation of the memory storage device proceeds (Col. 5, lines 52-56). Once normal operation of the memory is underway, the BIST unit 120 is not utilized. Therefore, there is no need for control signals being transmitted to the third logic section (which is not present in Irrinki). Lattimore does not add anything that would enable Irrinki to have two control signals, as recited in independent claim 13.

Since Irrinki does not teach or suggest a first logic section, a plurality of second logic sections and a plurality of third logic sections, and the addition of Lattimore does not provide Irrinki with a first logic section, a second logic sections and a third logic sections, the combination cannot teach or suggest transmitting to the SUT from the first logic section, when the first logic section is coupled to the SUT via the third logic section, one or more test-related signals; and transmitting to the SUT from the second logic section, when the second logic section is coupled to the SUT via the third logic section, one or more other signals to the SUT, as recited in independent claim 10.

Accordingly, since the (improper) combination of Irrinki and Lattimore does not teach or suggest the invention recited in independent claim 13, independent claim 13 is allowable over the combination, and the rejection of independent claim 13 under 35 U.S.C. §103(a) should be withdrawn.

Claims 14-21 depend from independent claim 13 and are allowable for at least the same reasons as independent claim 13.

Independent claim 22 recites a method of using a testing system that may be used to test a plurality of systems-under-test, the testing system including a first logic section, a plurality of second logic sections, and a plurality of third logic sections, each respective third logic section being coupled to the first logic section and to a respective second logic section, the method comprising:

configuring each respective third logic section to selectively couple ~~one of~~ the first logic section or the respective second logic section to a respective system-under-test based upon a respective control signal from the first logic section and also based upon

another control signal, the another control signal being transmitted to each third logic section from a source that is external to the plurality of systems-under-test, the first logic section, the plurality of second logic sections, and the plurality of third logic sections;

transmitting from the first logic section, when the first logic section is coupled to the respective SUT, one or more test-related signals to the respective SUT; and

transmitting from the respective second logic section, when the respective second logic section is coupled to the respective SUT, one or more respective other signals to the respective SUT.

As set forth above with regard to independent claim 10, Irrinki does not teach a first logic section, a second logic section and a third logic section. It follows then, that Irrinki does not teach a plurality of second logic sections and a plurality of third logic sections. The multiplexers 250, 252 that the examiner states correspond to the third logic circuit in the claim are actually part of the control block 130, which the examiner states corresponds to the second logic section. If the multiplexers are the third logic section, as suggested by the examiner, then Irrinki does not teach a second logic section. If the examiner believes that the control block 130 corresponds to the second logic section, then Irrinki also does not teach a third logic section that selectively couples the first logic section or the respective second logic section to the respective system-under-test based upon two control signals, as recited in the claim. Lattimore does not add anything that would enable Irrinki to have a first logic section, a plurality of second logic sections and a plurality of third logic sections, as recited in independent claim 22.

Furthermore, Irrinki does not teach two control signals. The BIST unit 120 of Irrinki begins its test algorithm when power is applied to memory storage device 100 to verify the operation of memory array 140 (Col. 5, lines 20-22). After the BIST unit 120 has completed testing, it becomes inactive and normal operation of the memory storage device proceeds (Col. 5, lines 52-56). Once normal operation of the memory is underway, the BIST unit 120 is not utilized. Therefore, there is no need for control signals being transmitted to the third logic section (which is not present in Irrinki). Lattimore does not add anything that would enable Irrinki to have two control signals, as recited in independent claim 22.

Since Irrinki does not teach or suggest a first logic section, a plurality of second logic sections and a plurality of third logic sections, and the addition of Lattimore does not provide Irrinki with a first logic section, a plurality of second logic sections and a plurality of third logic sections, the combination cannot teach or suggest transmitting from the first logic section, when the first logic section is coupled to the respective SUT, one or more test-related signals to the respective SUT; and transmitting from the respective second logic section, when the respective second logic section is coupled to the respective SUT, one or more respective other signals to the respective SUT, as recited in independent claim 22.

Accordingly, since the (improper) combination of Irrinki and Lattimore does not teach or suggest the invention recited in independent claim 22, independent claim 22 is allowable over the combination, and the rejection of independent claim 22 under 35 U.S.C. §103(a) should be withdrawn.

Claims 23 and 24 depend from independent claim 10 and are allowable for at least the same reasons as independent claim 22.

Based on the foregoing, applicants respectfully assert that claims 1-24 are allowable over the art of record and respectfully request that a timely Notice of Allowance be issued in this application.

In the event the Patent Office deems personal contact desirable in disposition of this matter, the Office is invited to contact the undersigned attorney at (508) 293-7835.

Please charge any fees occasioned by this submission to Deposit Account No. 05-0889.

Respectfully submitted,

Dated: 11/16/04

Scott A. Ouellette, Esq. (Reg. No. 38,573)
EMC Corporation
Office of the General Counsel
176 South Street
Hopkinton, MA 01748
Tel: 508-293-7835
Fax: 508-293-7189